WHAT IS CLAIMED IS:

1. A method for fabricating a storage capacitor comprising:

forming an initial deep trench structure through an etching process;

forming a sacrificial doped silicon layer extending from a surface of the interior of said deep trench into the silicon substrate, wherein a boundary is established between said doped sacrificial silicon layer and said silicon substrate;

selectively removing said sacrificial doped silicon layer from said trench interior surface;

fabricating a buried plate electrode;

fabricating a capacitor dielectric; and

fabricating a top electrode.

2. The method of claim 1, wherein said sacrificial doped silicon layer comprises p-doped silicon.

3. The method of claim 2, wherein said selectively removing said sacrificial doped silicon layer further comprises chemical etching using an aqueous solution of hydroxide.

4. The method of claim 2, wherein said p-doped silicon layer is formed by gas phase doping.

5. The method of claim 2, wherein said selectively removing said sacrificial doped silicon layer further comprises:

forming an n-type region extending from said internal p-type silicon interface further into said silicon substrate; and

selectively etching said p-type layer such that said n-type region remains substantially unetched during said selectively etching said p-type layer.

6. The method of claim 5, wherein said selectively etching said p-type layer comprises:

exposing said p-type layer to an aqueous solution of hydroxide;

applying a positive bias of about 1.2V between a counter electrode and a backside of a wafer containing said p-type layer; and

maintaining the positive bias for a duration sufficient to entirely remover said p-type layer.

7. The method of claim 5, wherein said p-type layer is formed by gas-phase doping.

8. The method of claim 6, wherein said p-type layer is formed by gas-phase doping.

9. The method of claim 1, wherein formation of said initial deep trench structure additionally comprises forming an etch-resistant collar located on a surface of the trench interior in a top region of said trench.

10. An array of DRAM trench capacitors, wherein each trench capacitor has a bottle shaped trench cross-section of substantially uniform shape when viewed in cross-section, and wherein the uniformity of bottle trench dimensions does not vary substantially among capacitors within the array.

11. The array of claim 10, wherein the steps for forming the array include:

forming an initial deep trench structure in a silicon substrate through an etching process;

forming a sacrificial doped silicon layer extending from a surface of an interior of said deep trench into the silicon substrate, resulting in an internal p-type silicon/silicon interface;

selectively removing said sacrificial doped silicon layer from said trench interior surface; and

forming a buried plate electrode, capacitor dielectric, and top electrode.

12. The array of claim 11, wherein said sacrificial doped silicon layer comprises p-doped silicon.

13. The array of claim 12, wherein said p-doped silicon layer is formed by gas phase doping.

14. The array of claim 11, wherein said selectively removing said sacrificial doped silicon layer comprises:

forming an n-type region extending from said internal p-type silicon interface further into said silicon substrate; and

selectively etching said p-type layer such that said n-type region remains substantially unetched during said selectively etching said p-type layer.

15. The array of claim 14, wherein said selectively etching said p-type layer is performed by chemical etching using an aqueous solution of hydroxide of potassium or ammonia, further comprising the step of applying a bias voltage to said p-type layer during said chemical etching.

16. A method for fabricating bottle-shaped etched structures in silicon, comprising:

forming an initial narrow etched region by a directional silicon etching process;

forming an etch-resistant collar in the top portion of the etched region;

forming a sacrificial doped silicon layer extending from a surface of an interior of said etched region further into said silicon, wherein said sacrificial doped silicon layer is fabricated by gas phase doping of said silicon; and

selectively removing said sacrificial doped silicon layer by etching in a chemical solution.

17. The method of claim 16, wherein said selectively removing said sacrificial doped silicon layer further comprises:

forming an n-type region extending from said internal p-type silicon interface further into said silicon substrate; and

selectively etching said p-type layer such that said n-type region remains substantially unetched during said selectively etching said p-type layer.

18. The method of claim 17, wherein said selectively etching said p-type layer comprises:

exposing said p-type layer to an aqueous solution of hydroxide;

applying a positive bias of about 1.2V between a counter electrode and a backside of a wafer containing said p-type layer; and

maintaining the positive bias for a duration sufficient to entirely remover said p-type layer.